AMENDMENTS TO THE CLAIMS:

1. (Canceled)

2. (Currently amended) An input circuit comprising:

a data input means for receiving input data of the input circuit;

a data latch means for latching output data of the input circuit;

a reset means for resetting the data latch means in response to a first logic level of a first clock signal;

a latch enhancement means for enhancing a latching operation of the data latch means in response to a first logic level of a second clock signal that is delayed in a phase from the first clock signal; and

a clock synchronization means for transferring the input data from outputs of the data input means to the data latch means in response to a second logic level of the first clock signal,

the clock synchronization means blocking a feedthrough current that flows through the reset means, the data latch means, and the latch enhancement means when the first and second clock signals are in a state of said first logic level ~~state~~.

3. (Currently amended) An input circuit comprising:

a data input means for receiving input data of the input circuit;

a data latch means connected to the data input means and including an activating means for activating the data latch means and inputting the input data in response to a first logic level of a first clock signal;

a reset means for resetting the data latch means in response to a second logic level of

the first clock signal; and

a latch enhancement means for enhancing a latching operation of the data latch means in response to a first logic level of a second clock signal that is delayed in a phase from the first clock signal,

wherein said activating means blocks a feedthrough current that flows through the reset means, the data latch means, and the latch enhancement means when the first clock signal is in a state of said second logic level ~~state~~ and the second clock signal is in a state of said first logic level ~~state~~.

4.-9. (Canceled)

10. (Currently amended) The input circuit of claim 2, wherein:

the data input means comprises sources of both a first NMOS transistor and a second NMOS transistor being connected to a power source ~~via said clock synchronization means~~;

a gate of the first NMOS transistor being connected to a first data input terminal;

a gate of the second NMOS transistor being connected to a second data input terminal;

a drain of the first NMOS transistor being connected to a common terminal at which one of a pair of complementary signals constituting the outputs of the input data means appears; and

a drain of the second NMOS transistor being connected to a common terminal at which another one of the pair of complementary signals constituting the outputs of the input data means appears.

11. (Currently amended) The input circuit of claim 2, wherein the clock synchronization means comprises gates of a first NMOS transistor and a second NMOS transistor being connected to a first clock input terminal; a source of the first NMOS transistor being connected~~, via said data input means,~~ to a first common terminal at which one of a pair of complementary signals constituting the outputs of the input data means appears; a source of the second NMOS transistor being connected~~, via said data input means,~~ to a second common terminal at which the other one of the pair of complementary signals constituting the outputs of the input data means appears; a drain of the first NMOS transistor being connected to a third common terminal; and a drain of the second NMOS transistor being connected to a fourth common terminal.

12. (Currently amended) The input circuit of claim 2, wherein:

the latch enhancement means comprises sources of both a first NMOS transistor and a second NMOS transistor being connected to a power source ~~via said clock synchronization means~~;

gates of both the first NMOS transistor and the second NMOS transistor being connected to a clock input terminal;

a drain of the first NMOS transistor being connected to a first common terminal at which one of a pair of complementary signals constituting the outputs of the ~~input~~ data input means appears; and

a drain of the second NMOS transistor being connected to a second common terminal at which another one of the pair of complementary signals constituting the outputs of the ~~input~~ data input means appears.

13-17. (Canceled)

18. (Currently amended) An input circuit comprising:

a data input unit that receives input data of the input circuit;

a data latch unit that latches output data of the input circuit;

a reset unit that resets the data latch unit in response to a first logic level of a first clock signal;

a latch enhancement unit that enhances a latching operation of the data latch unit in response to a first logic level of a second clock signal that is delayed in a phase from the first clock signal; and

a clock synchronization unit that transfers the input data from the outputs of the data input unit to the data latch unit in response to a second logic level of the first clock signal,

the clock synchronization unit blocking a feedthrough current that flows through the reset unit, the data latch unit, and the latch enhancement unit when the first and second clock signals are in a state of said first logic level ~~state~~.

19. (Currently amended) An input circuit comprising:

a data input unit that receives input data of the input circuit;

a data latch unit, connected to the data input unit, that latches output data of the input circuit, the data latch unit having an activating unit that activates the data latch unit and inputs the input data in response to a first logic level of a first clock signal;

a reset unit that resets the data latch unit in response to a second logic level of the first clock signal;

a latch enhancement unit that enhances a latching operation of the data latch unit in

response to a first logic level of a second clock signal that is delayed in a phase from the first clock signal,

wherein said activating unit blocks a feedthrough current that flows through the reset unit, the data latch unit, and the latch enhancement unit when the first clock signal is in a state of said second logic level ~~state~~ and the second clock signal is in a state of said first logic level ~~state~~.